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MS-7358 uATX **Version: 1.0**

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q35/G33 North Bridge
Intel ICH9 (DO/DH South Bridge)

On Board Device:

CLOCK Gen ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LPC TPM -- SLB9635
LAN -- INTEL NINEVEH/EKRON
HD Audio Codec -- ALC888
1394 Controller -- VT6308 (2-port)
PCIE to PATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4


Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT *1
PCI SLOT * 2

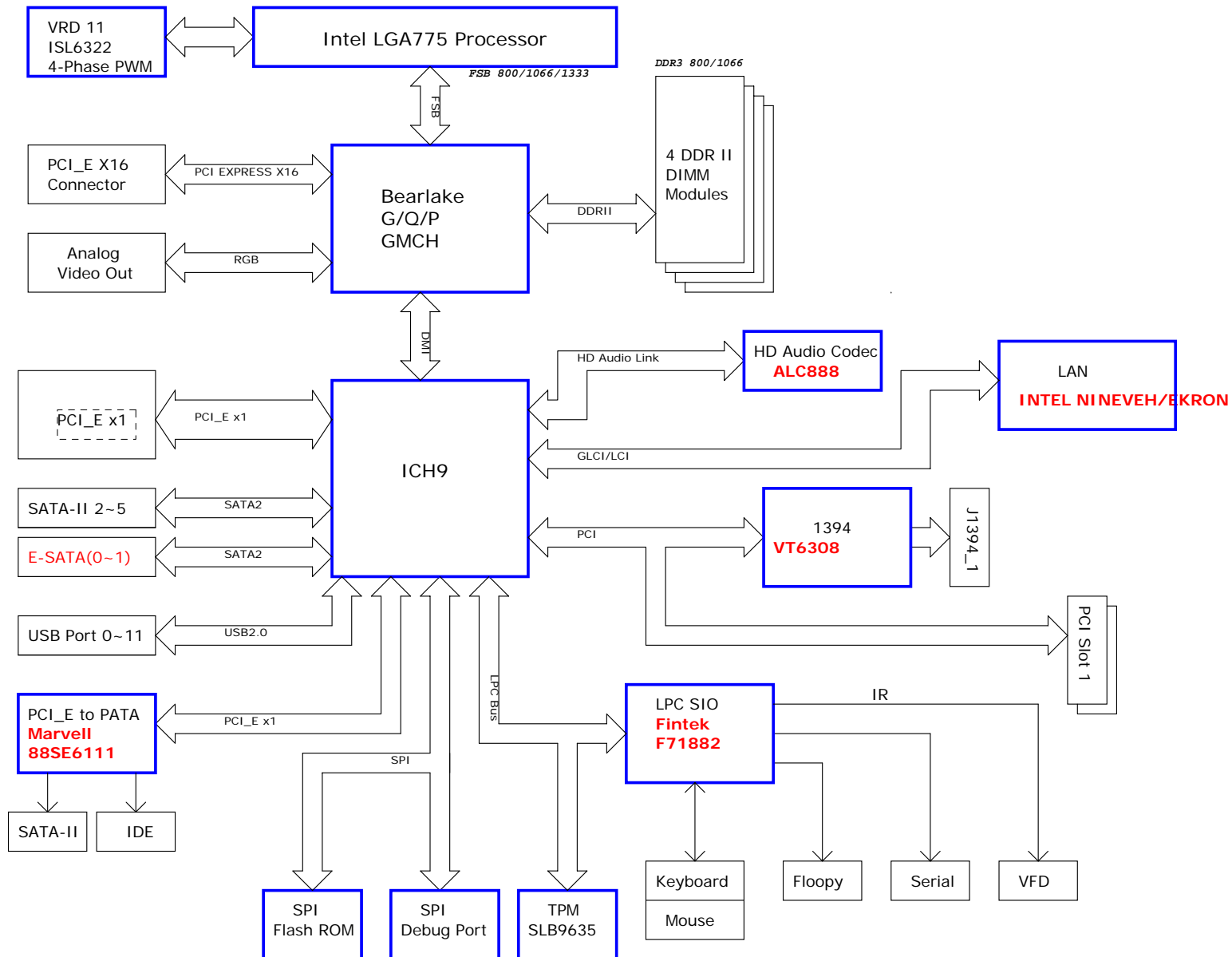
PWM: Intersil ISL6322 (4 Phases) w/ ISL6612 driver

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-Q33/ICH9DO	cfg-7358-STD	

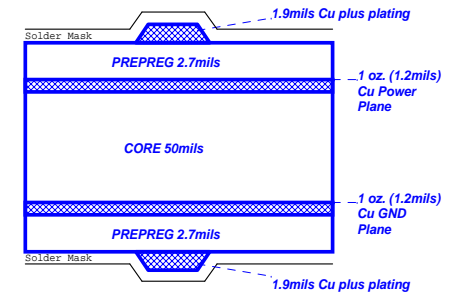
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				MS-7358			
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Block Diagram



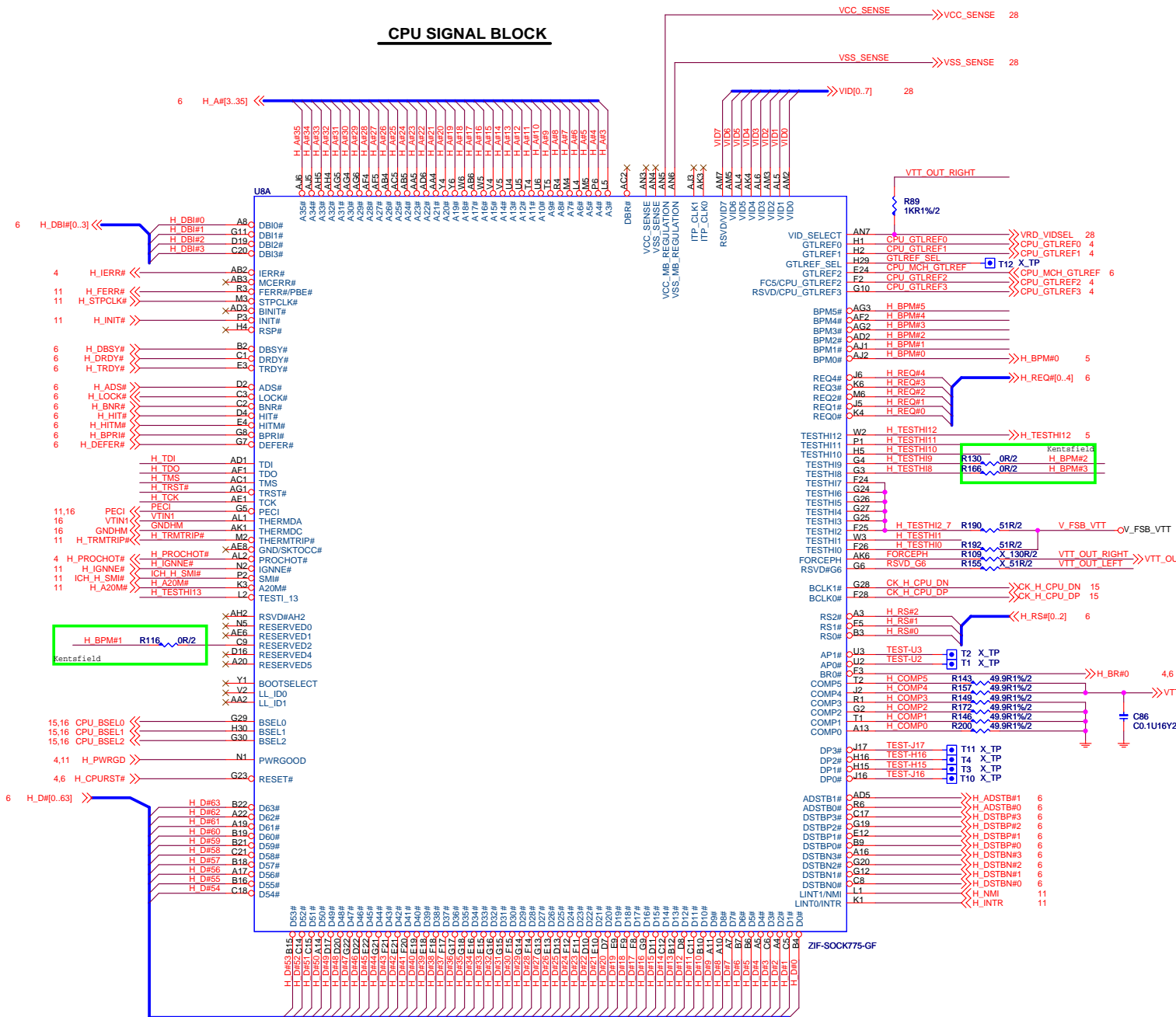
Board Stack-up

(1080 Prepreg Considerations)

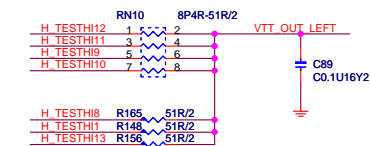
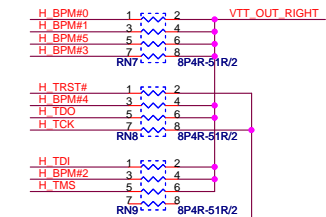
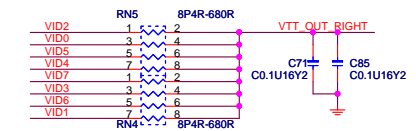


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

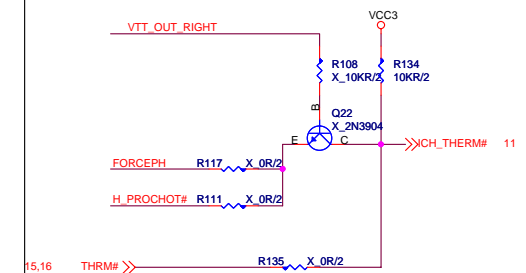
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



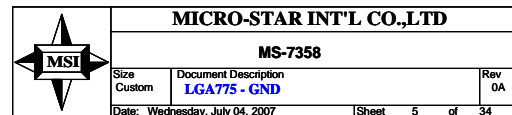
Thermal TRIP

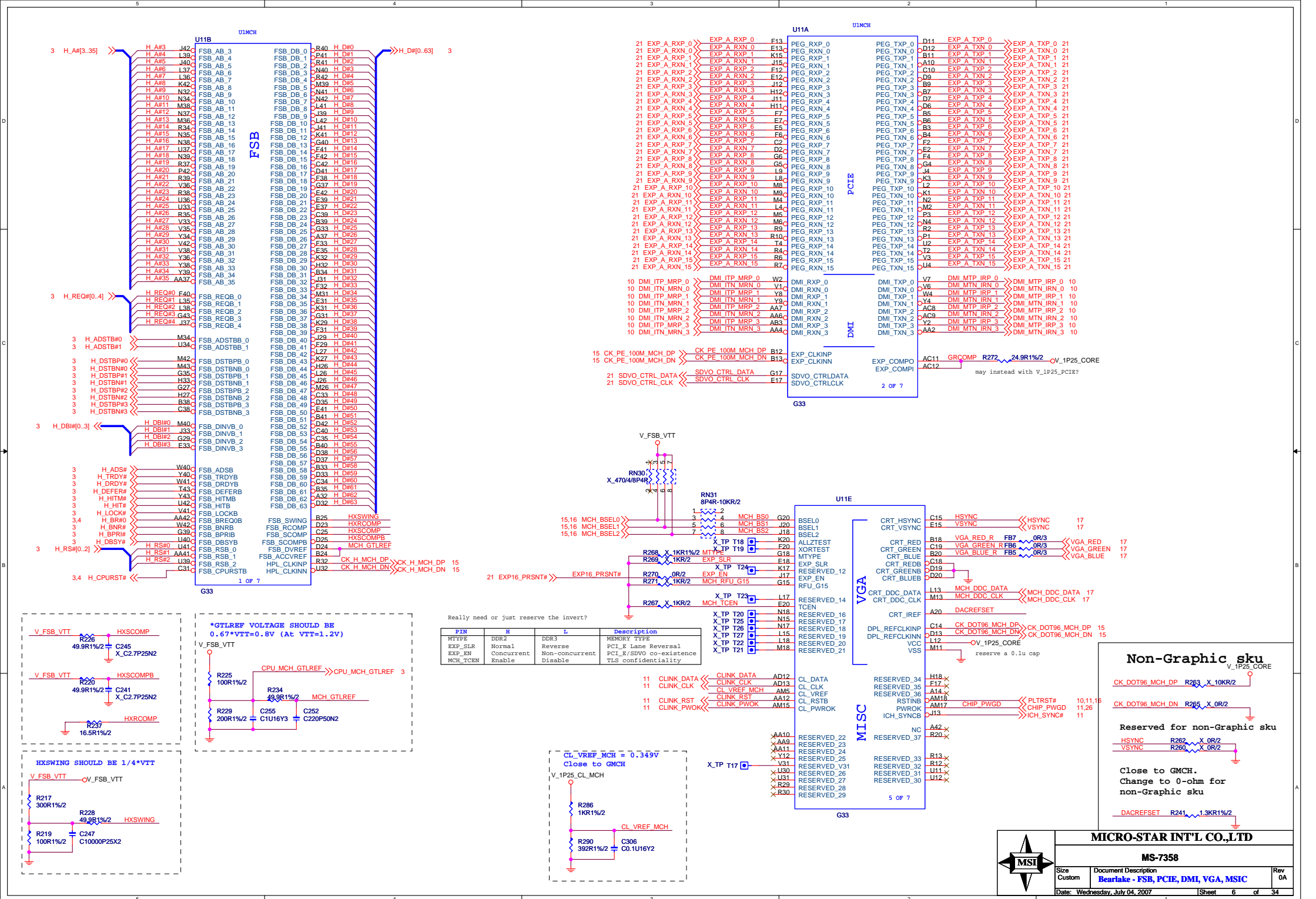


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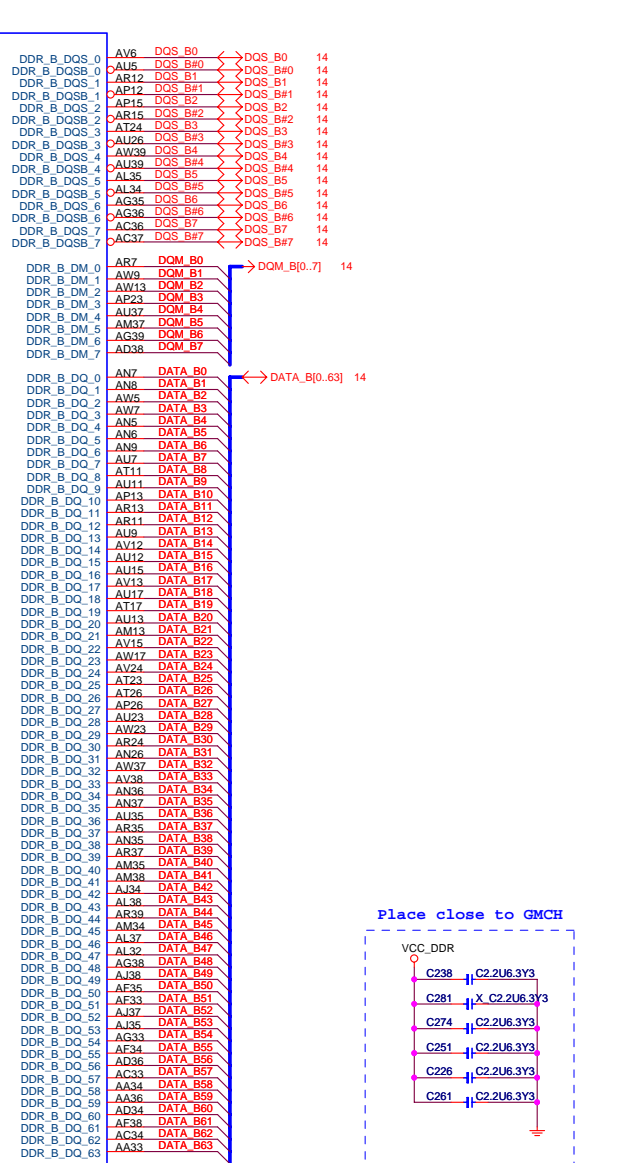
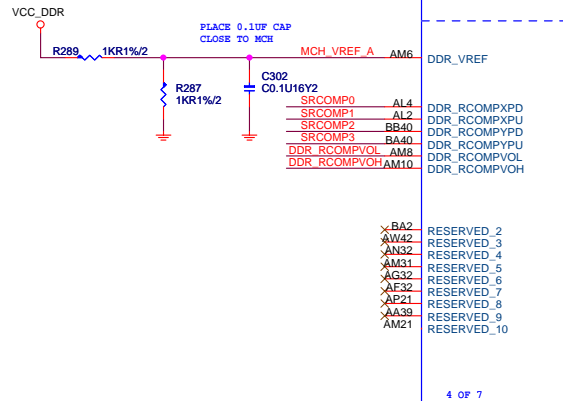
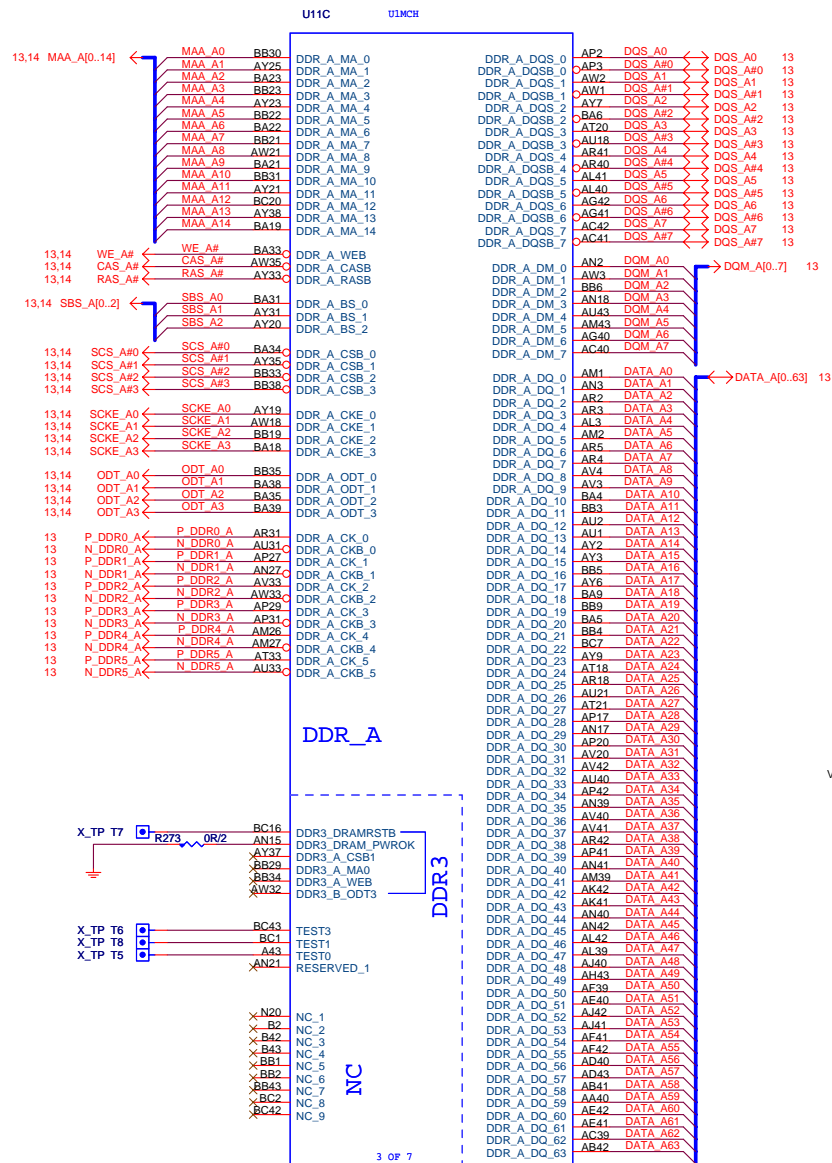




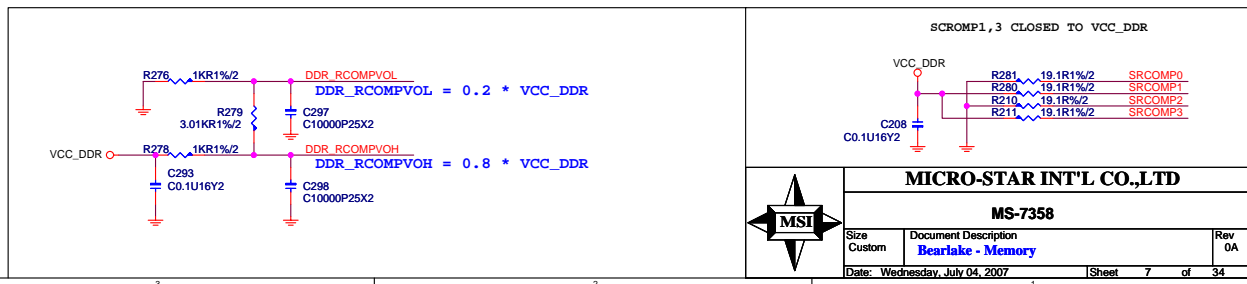
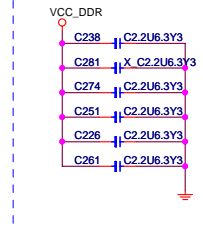
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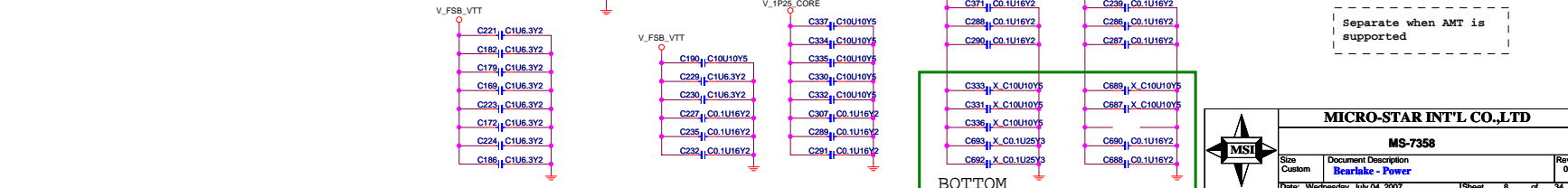
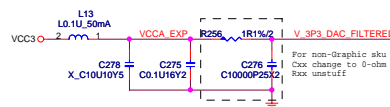


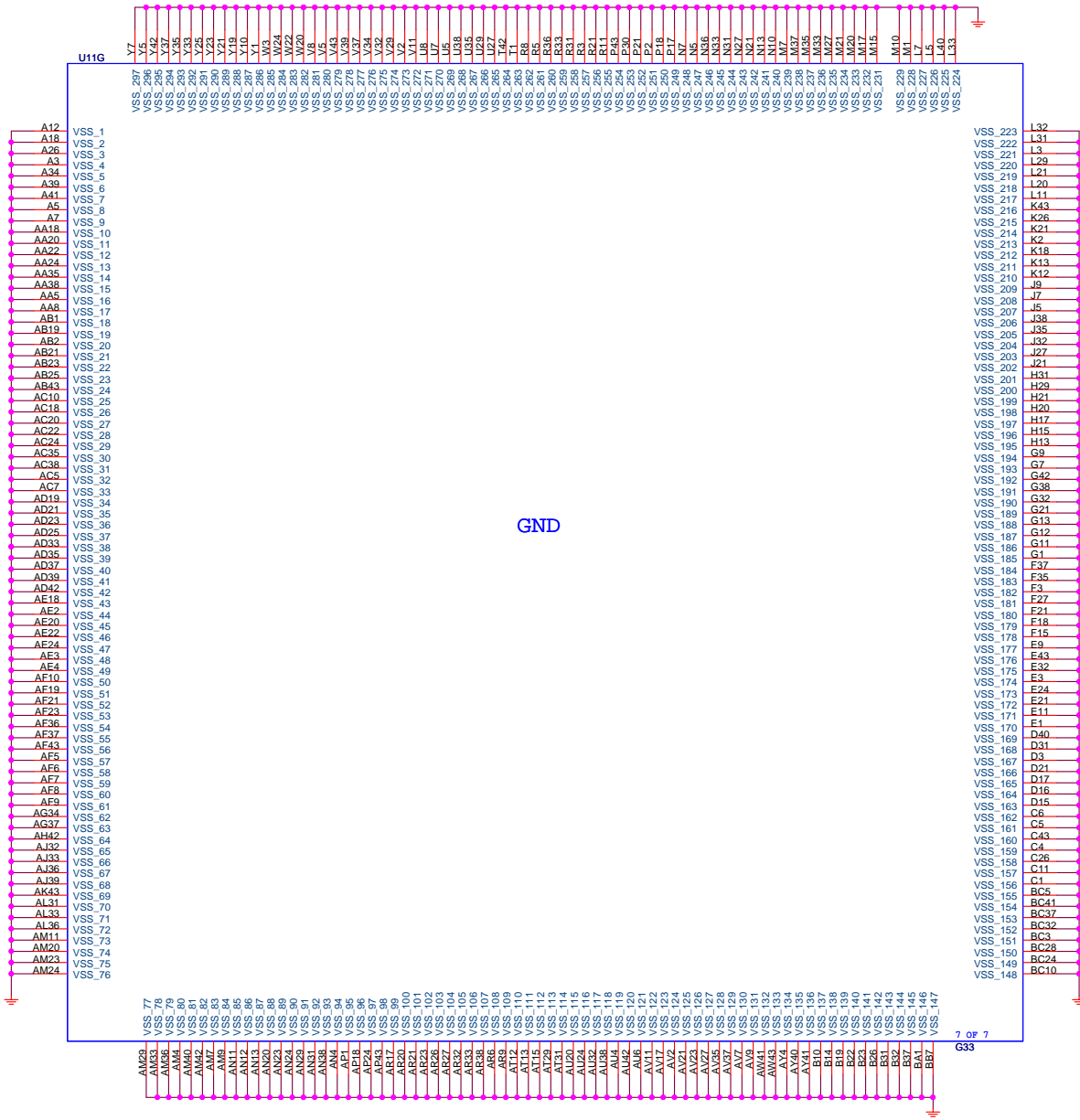
Place close to GMCH

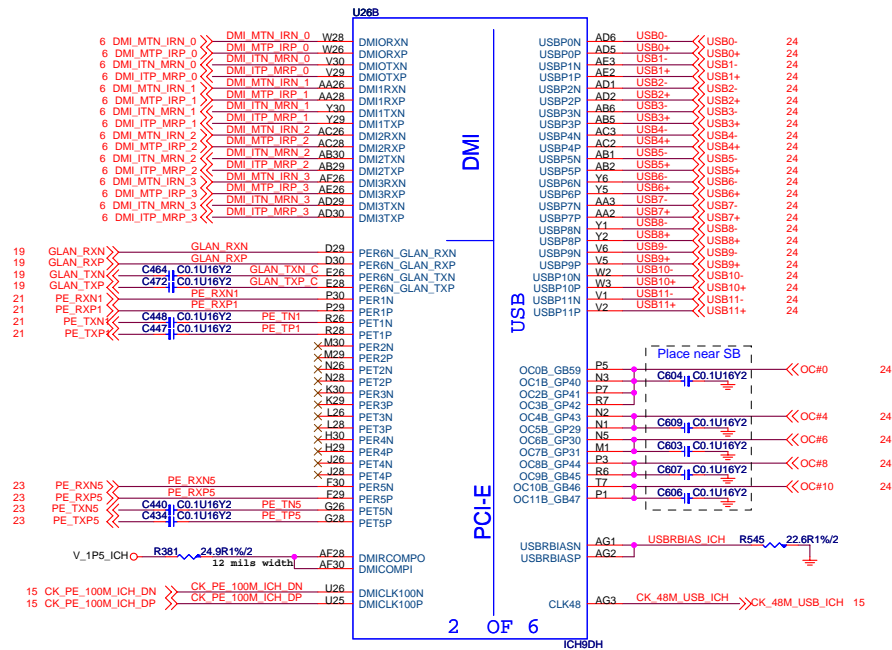
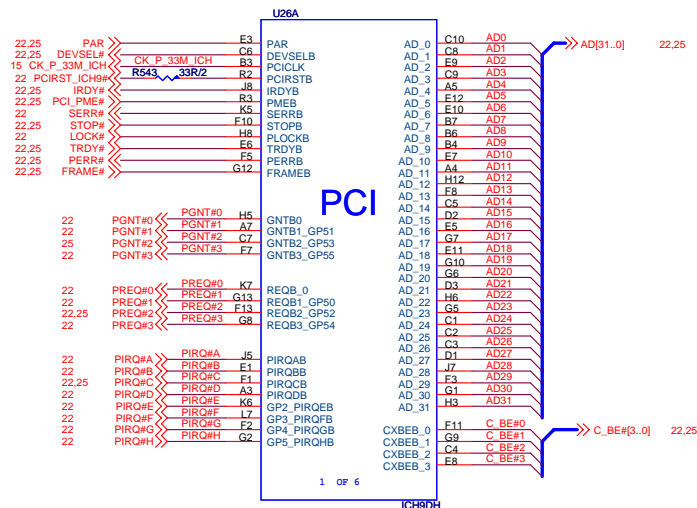


VCCD_CRT
For non-Graphic sku
change to 0-ohm (0402)

VCCDQ_CRT
For non-Graphic sku
change to 0-ohm (0603)







SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

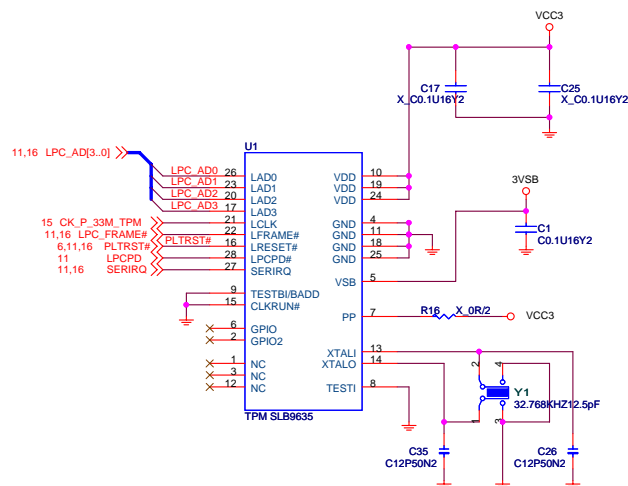
PGNT#(3:0) Internal Pull-up

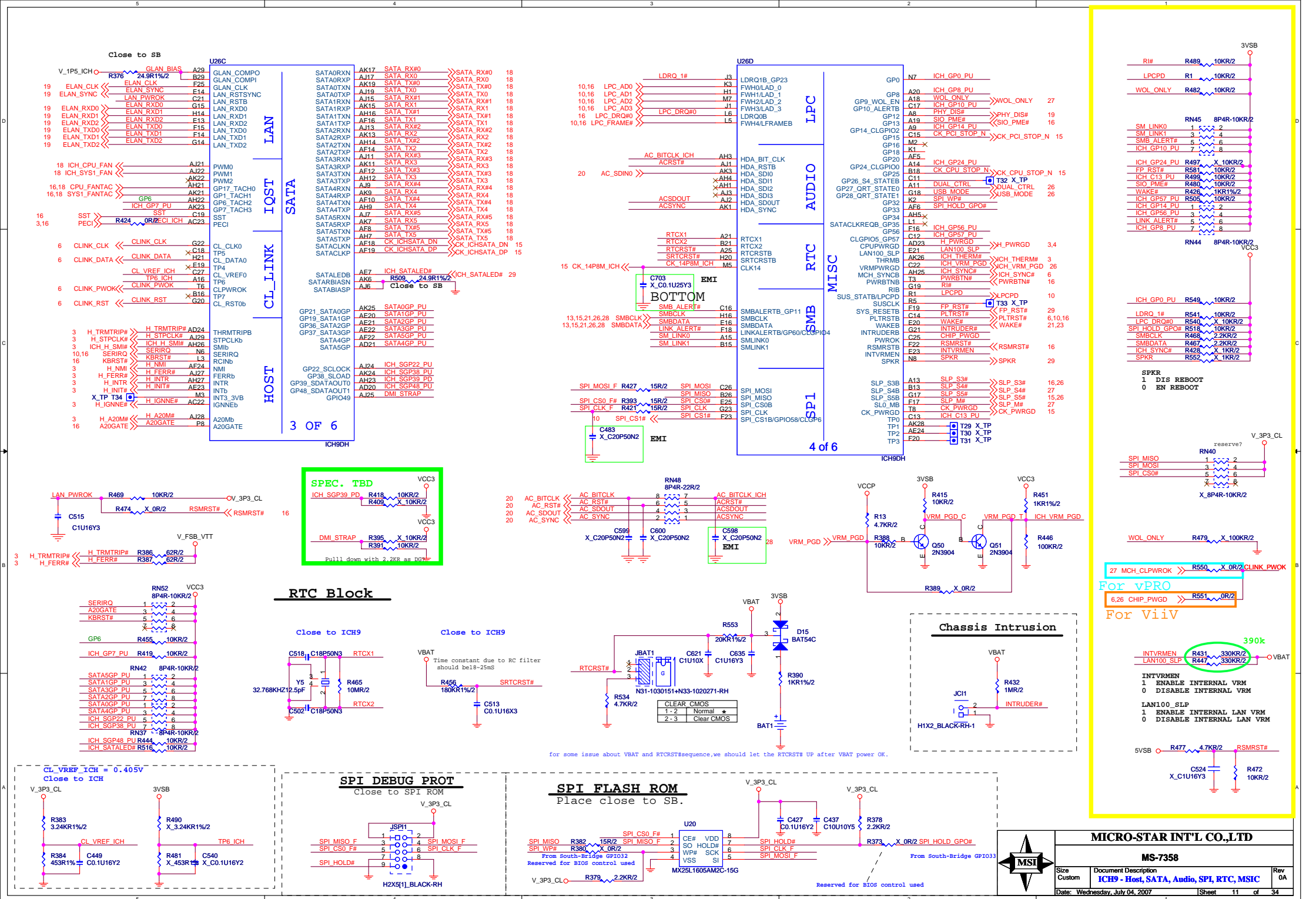


SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCI-E PORT CONFIG 2 BIT 0 (5-6)

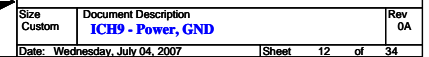
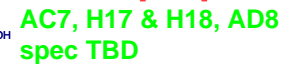
HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0]. Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X

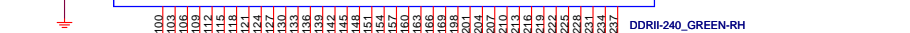
TPM - Security Controller





V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.

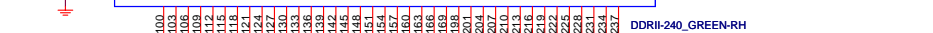




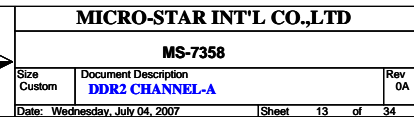
VCC_DDR

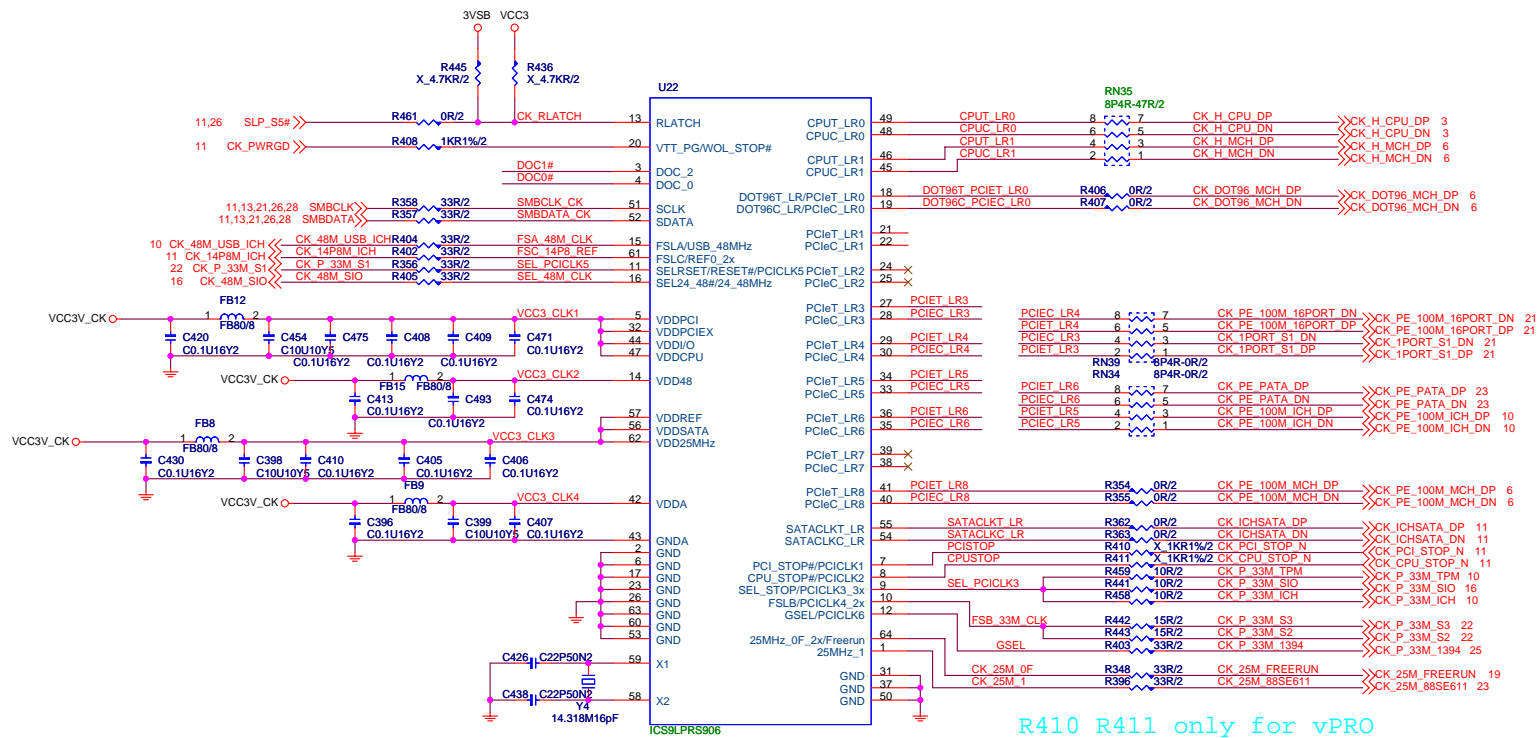
R282 1KR1%/2

DIMM_VREF A

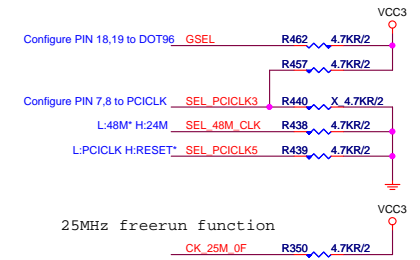


A	M

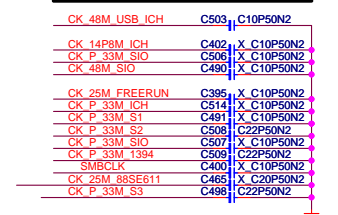




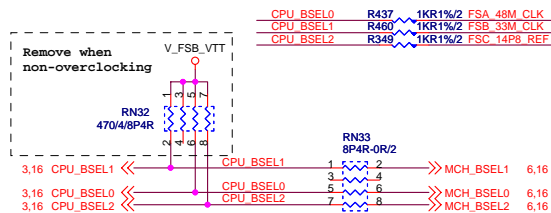
CLOCK GEN STRAPPING



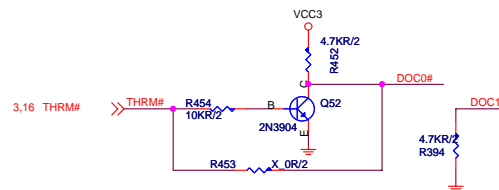
EMI



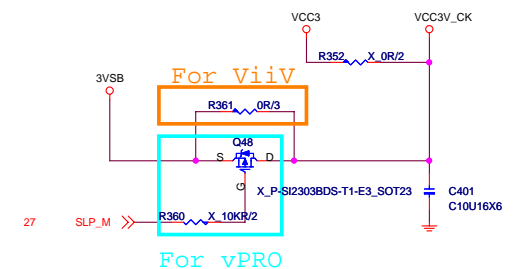
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz (1066)
0 0 1	133 MHz (533)
0 1 0	200 MHz (800)
1 0 0	333 MHz (1333)
1 1 0	400 MHz (1600)



D.O.T

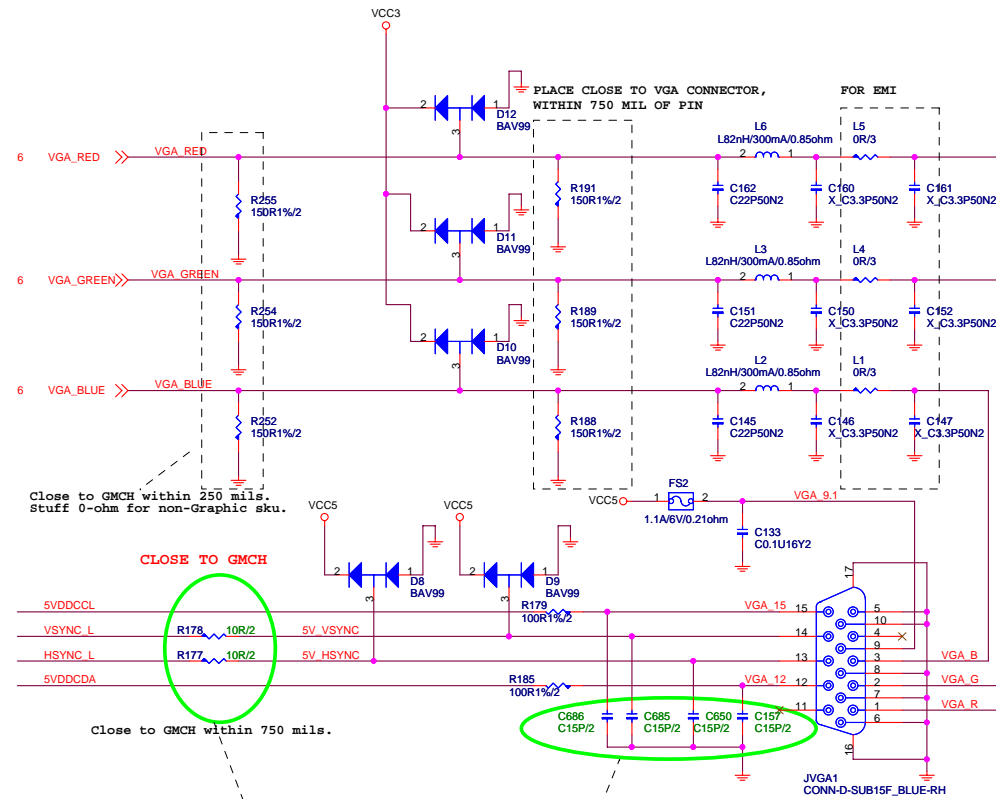
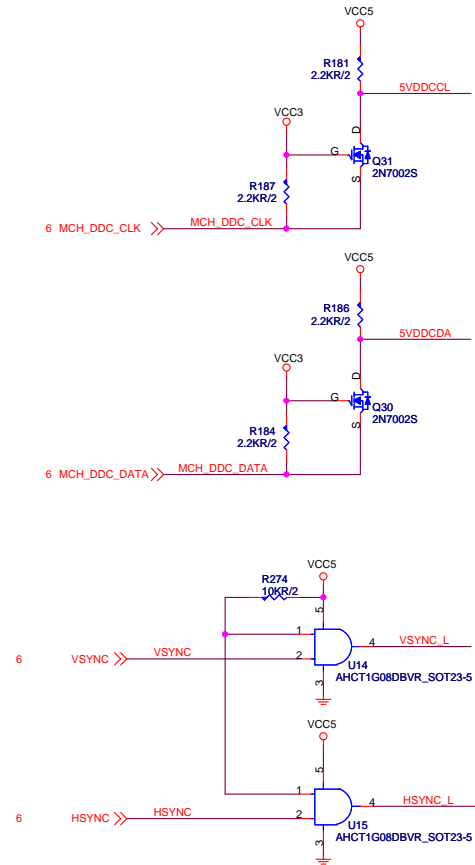


AMT POWER



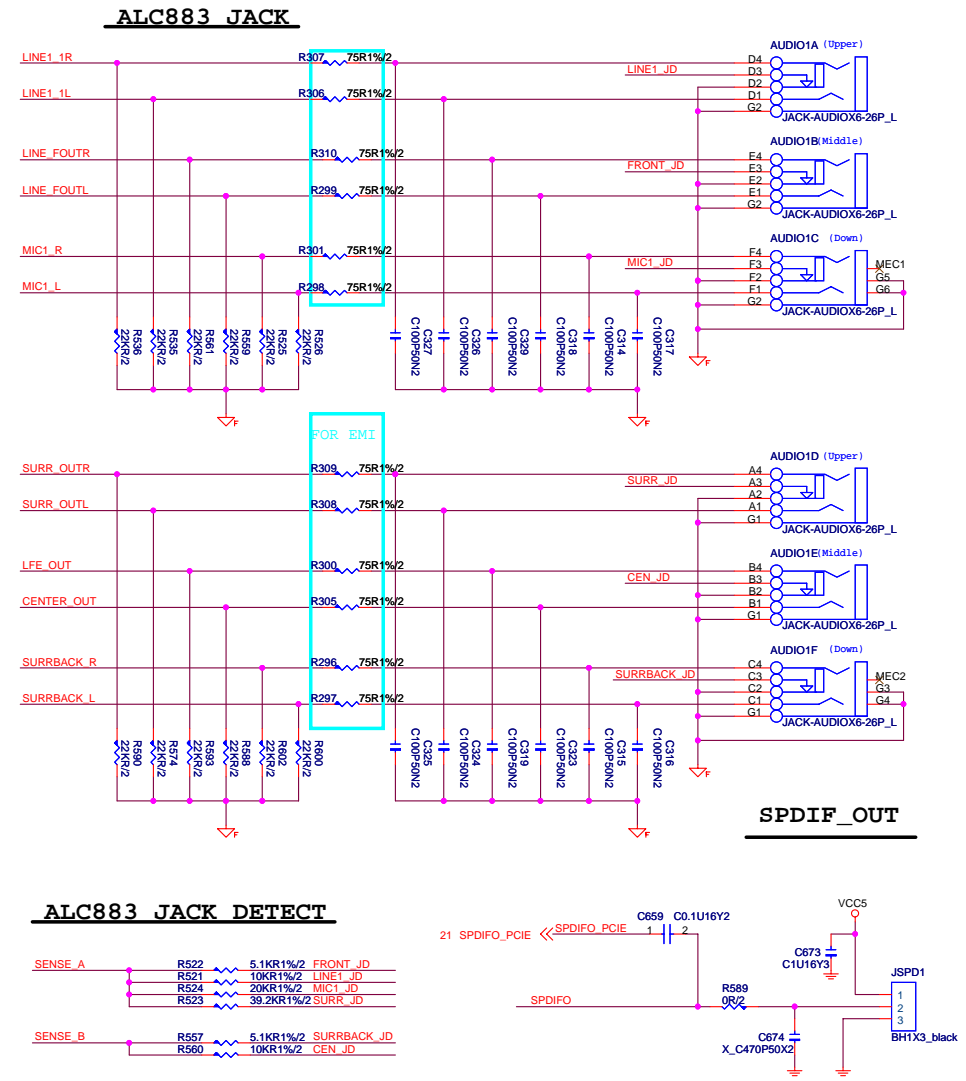
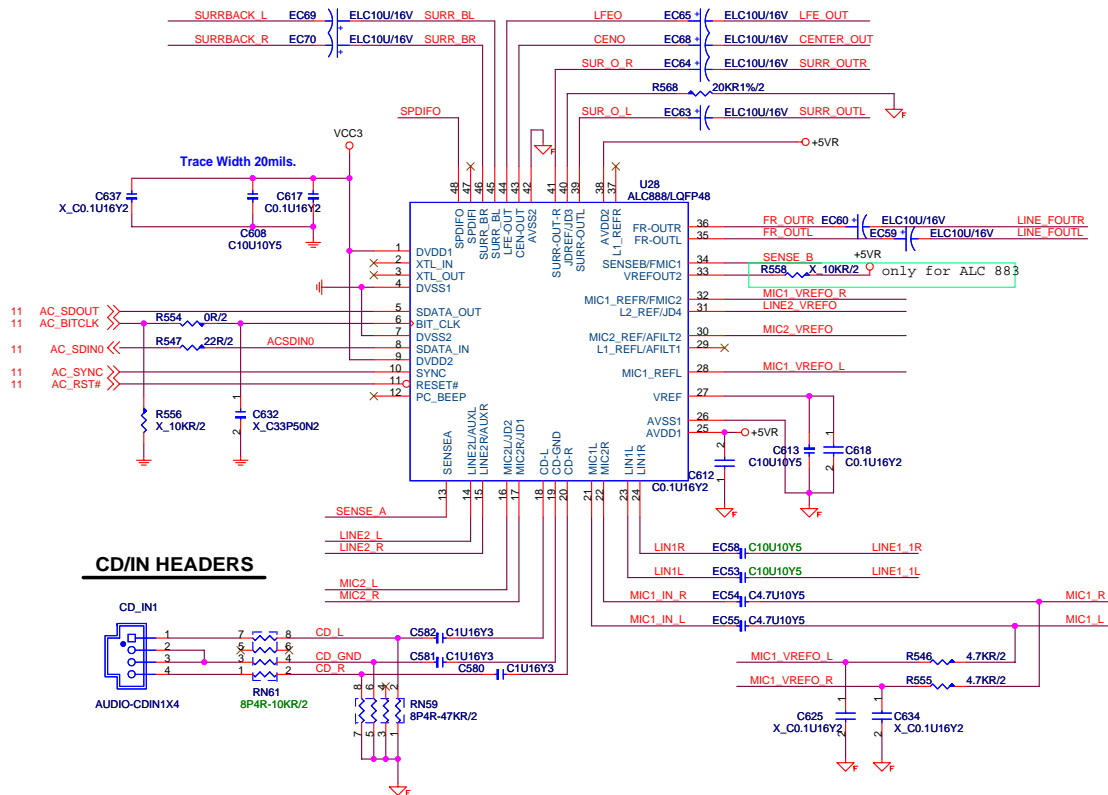
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Video Connector

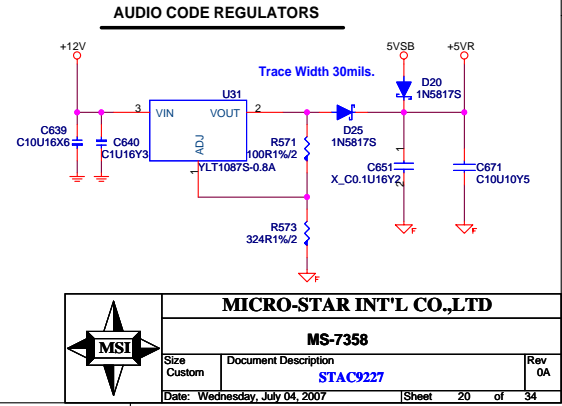
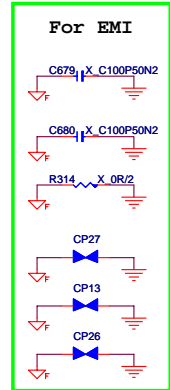
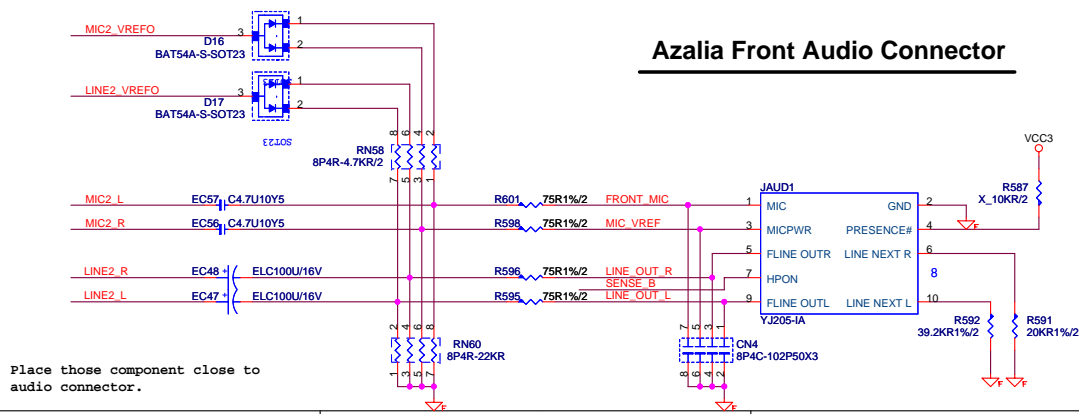


Modify HSYNC/VSYNC Circuit
 1. R178,R177 from 30R to 10R
 2. CN3 from 33p to 15p
 For Rise time edge not clean 07.3.30 by Robile

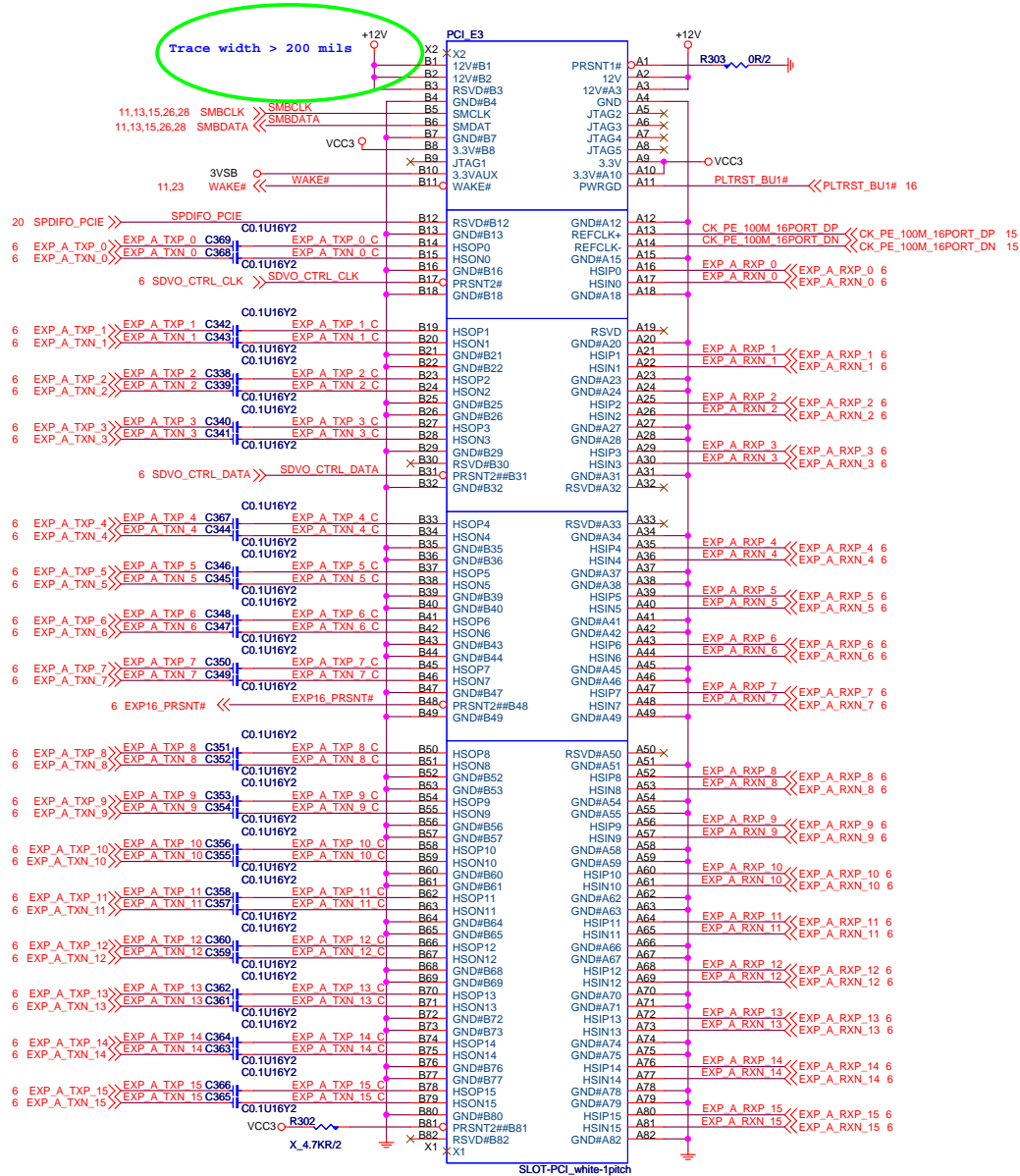
ALC883 CODEC



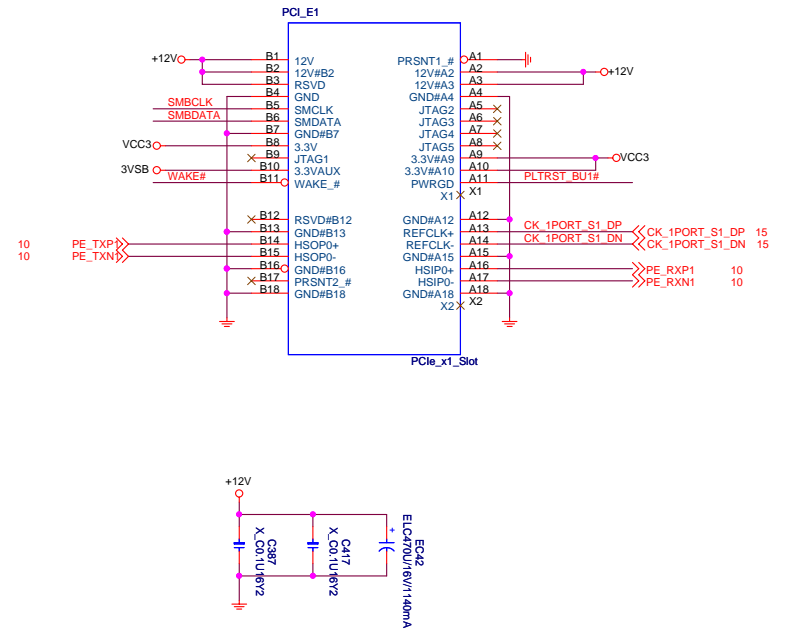
Azalia Front Audio Connector



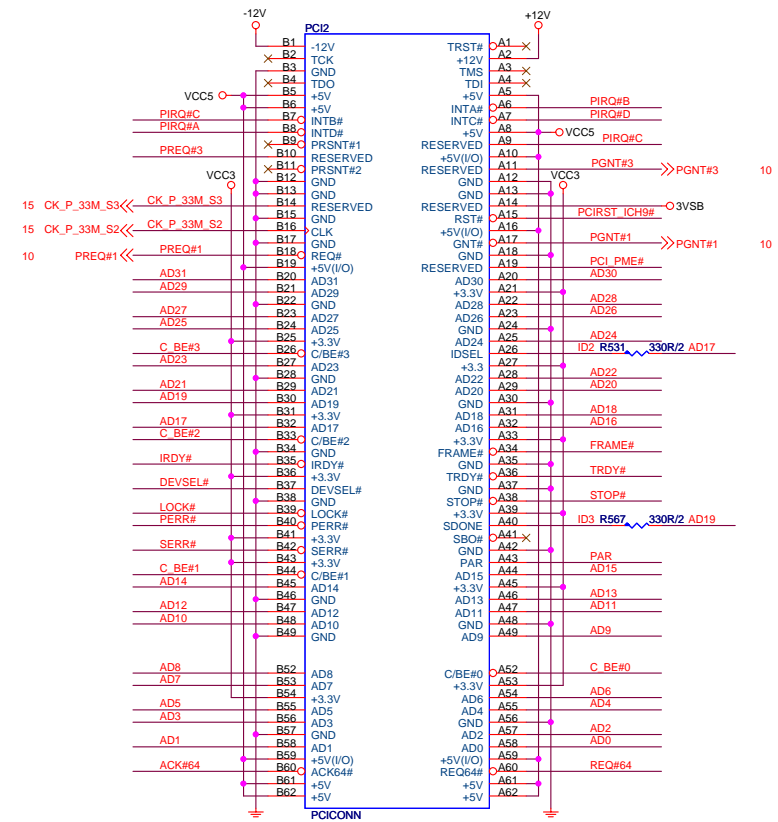
PCI_Express X16 Slot



PCI_Express X4 Slot (Share with PCI_E x1 Slots)



PCI SLOT 2 (PCI VER: 2.2 COMPLY)

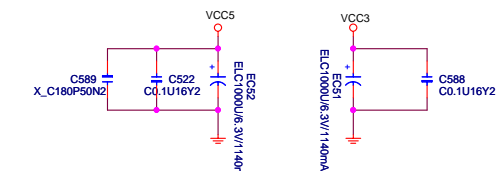


IDSEL = AD17

MASTER = PREQ#1

PIRQ#B

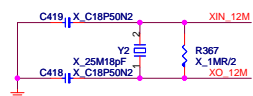
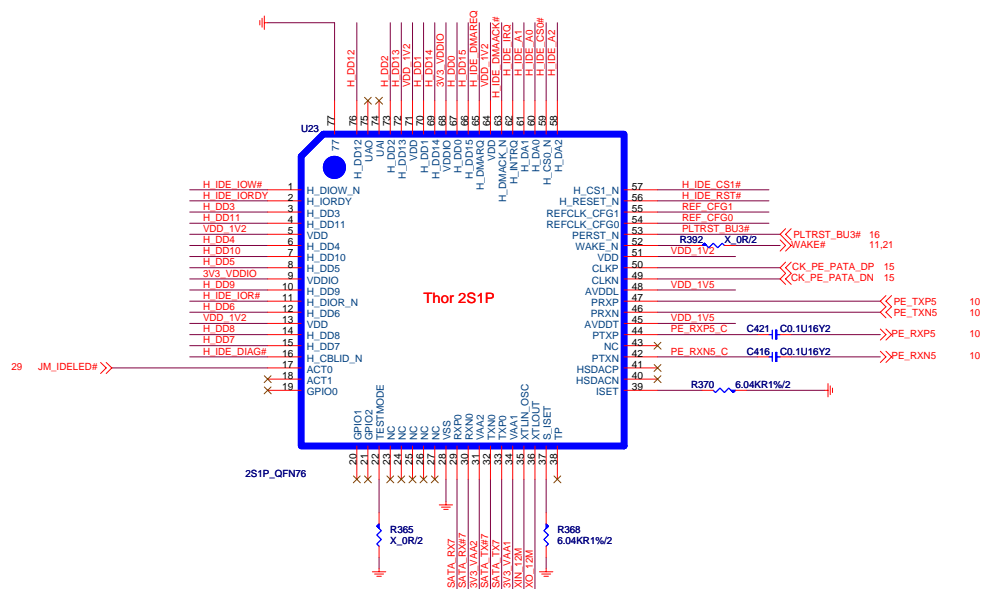
PCI SLOT DECOUPLING CAPACITORS



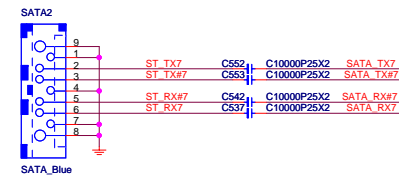
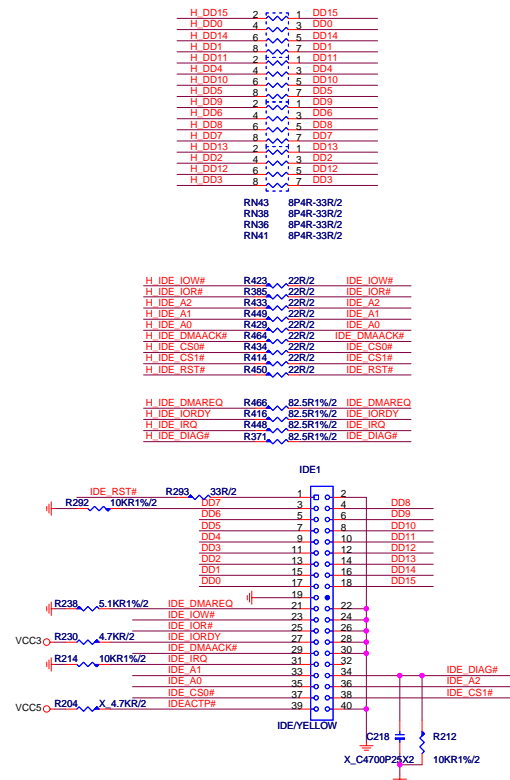
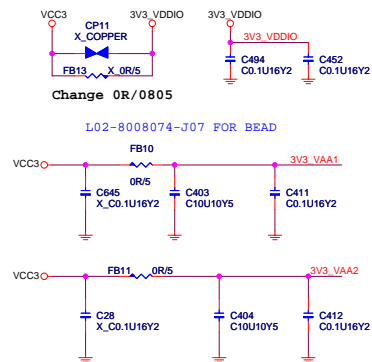
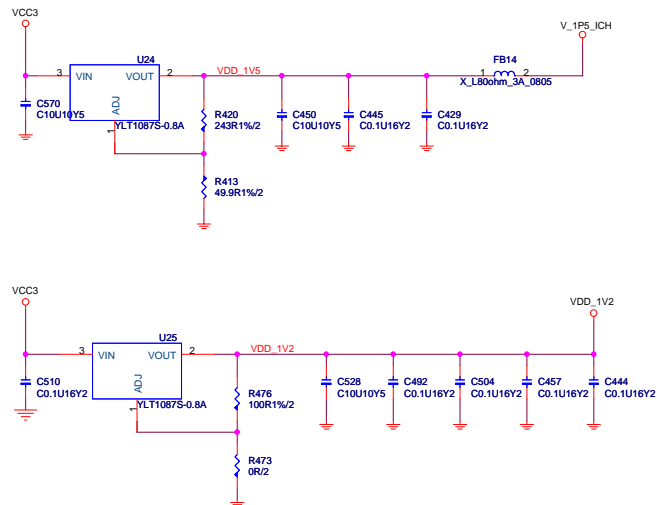
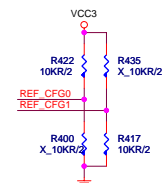
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Hi-Speed PCIE to SATA/PATA Bridge



```
REF_CFG[1:0] =  
00:20MHz  
01:25MHz
```



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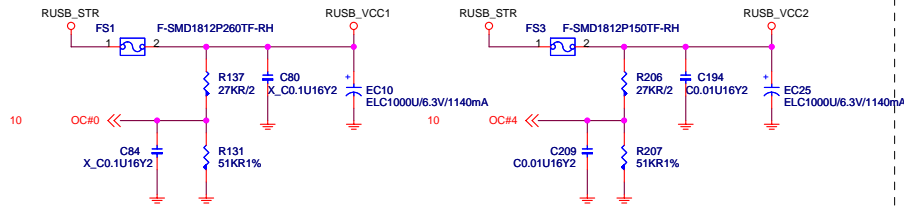
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Size	Document Description
Custom	Marvell 88SE6111 PCIe to PATA/SATA

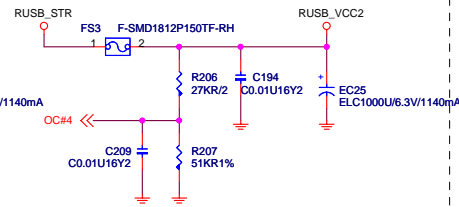
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Rear USB Connector

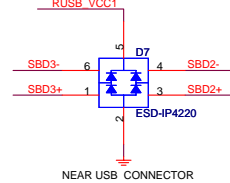
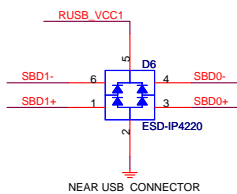
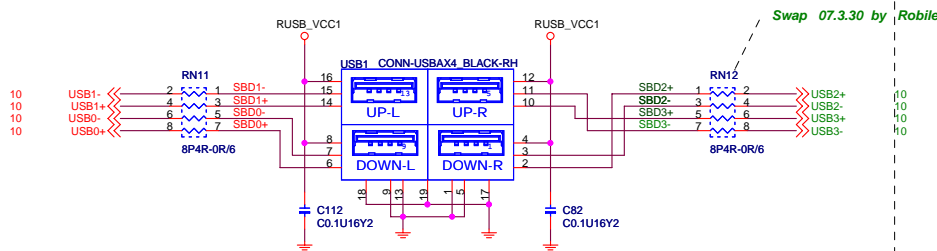
USB POWER FOR PORT 0,1 NEAR CONNECTOR



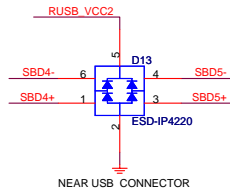
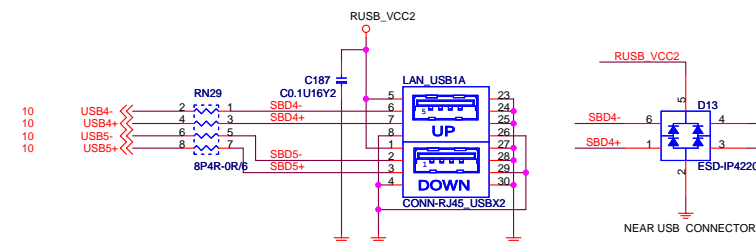
USB POWER FOR PORT 2,3,4,5 NEAR CONNECTOR



REAR USB PORT 0-3 (2x2)

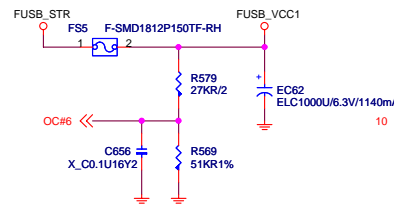


REAR USB PORT 4,5 (With LAN)

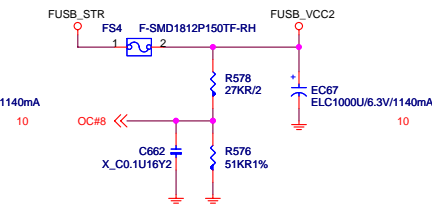


Front USB Connector

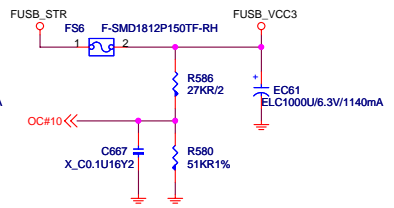
USB POWER FOR PORT 6,7 NEAR CONNECTOR



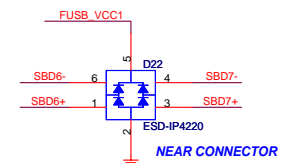
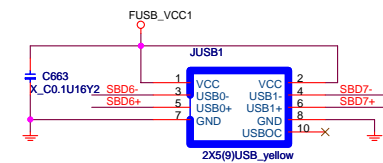
USB POWER FOR PORT 6,7 NEAR CONNECTOR



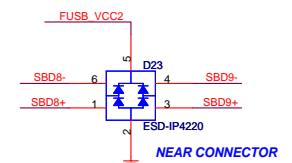
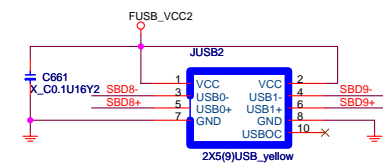
USB POWER FOR PORT 6,7 NEAR CONNECTOR



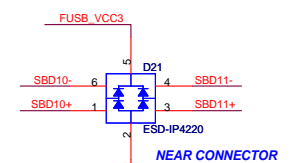
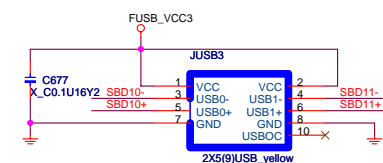
FRONT USB PORT 6,7



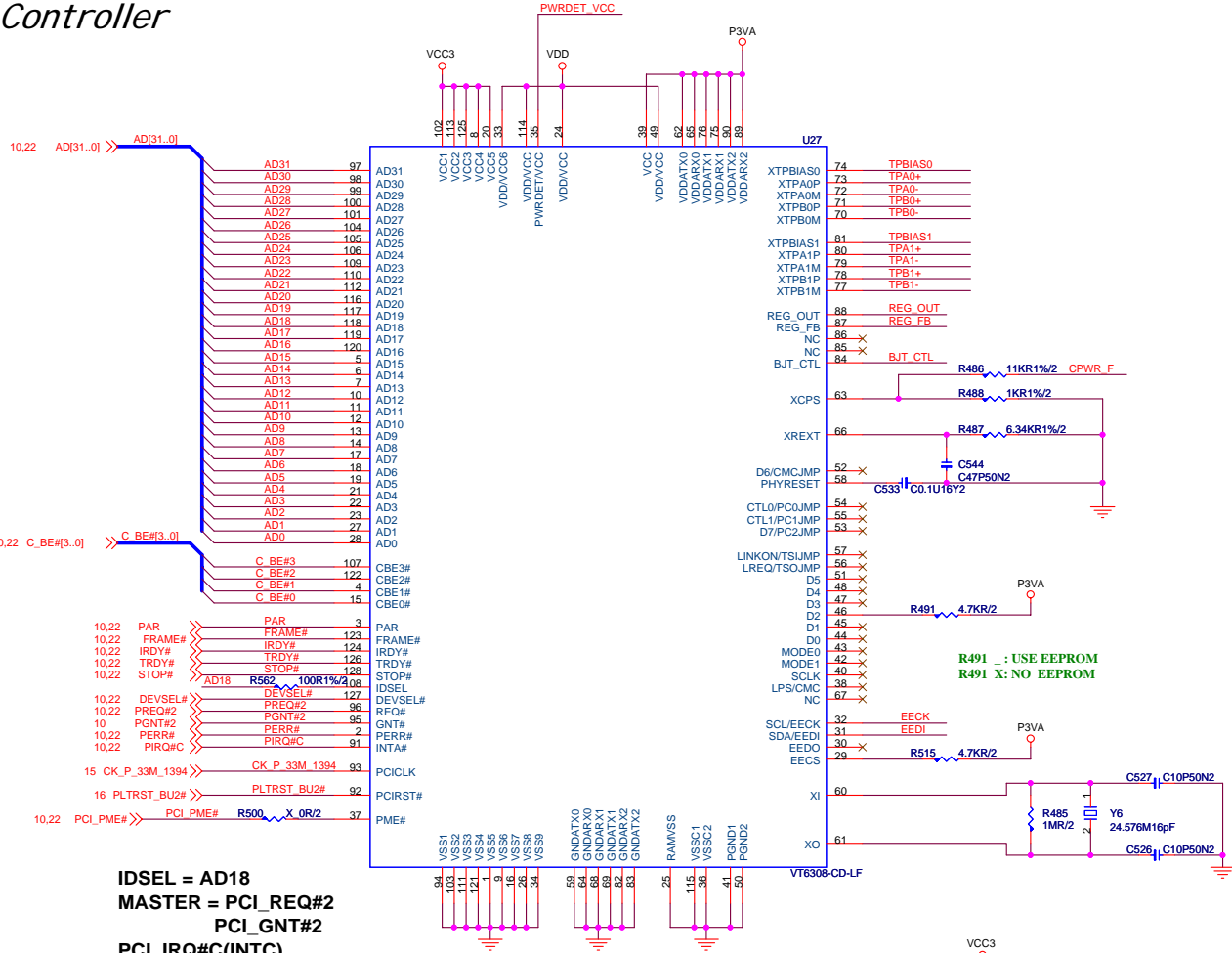
FRONT USB PORT 8,9



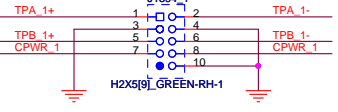
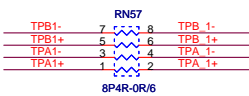
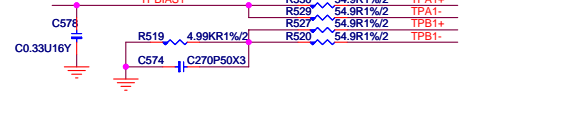
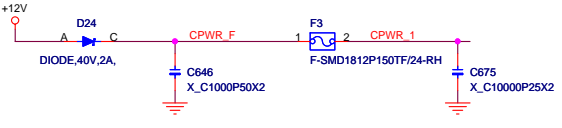
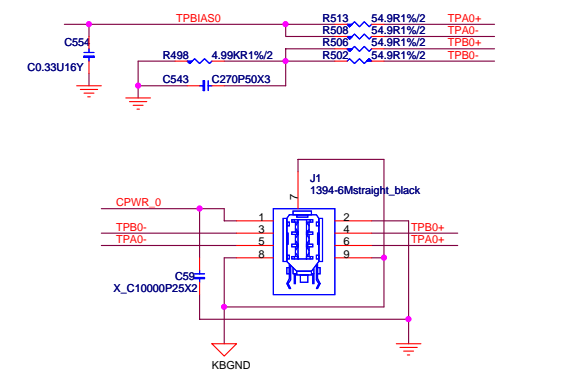
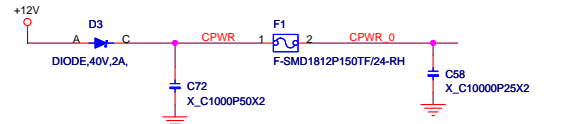
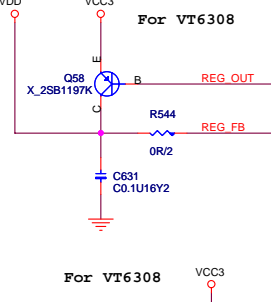
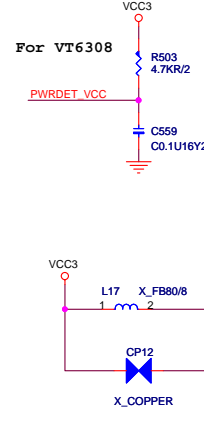
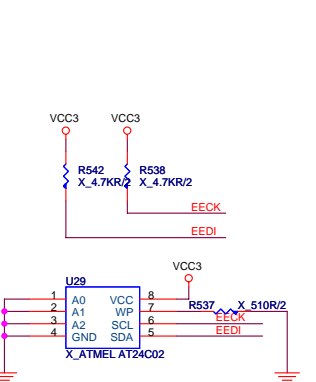
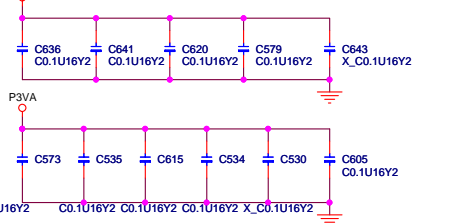
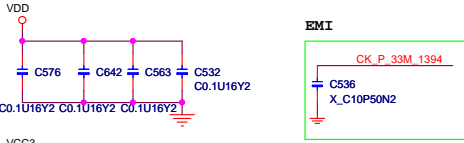
FRONT USB PORT 10,11



1394a OHCI Link Layer
Controller



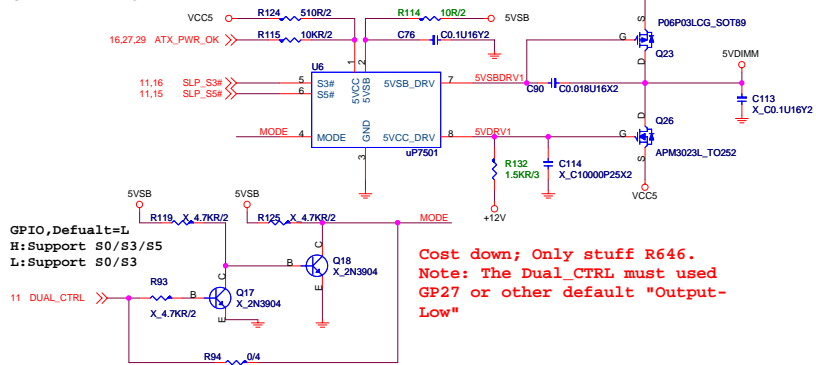
IDSEL = AD18
MASTER = PCI_REQ#2
PCI_GNT#2
PCI_IRQ#C(INTC)



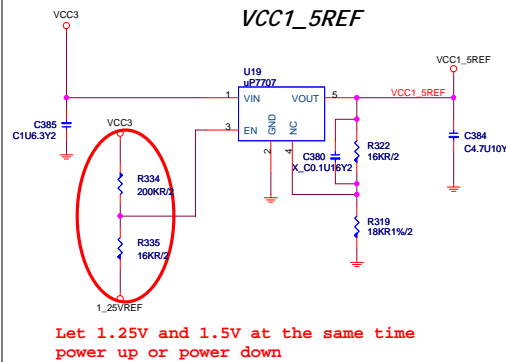
For Intel 1394 pinheader

MICRO-STAR INT'L CO.,LTD			
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Custom	IEEE-1394 VIA-VT6308	0A	
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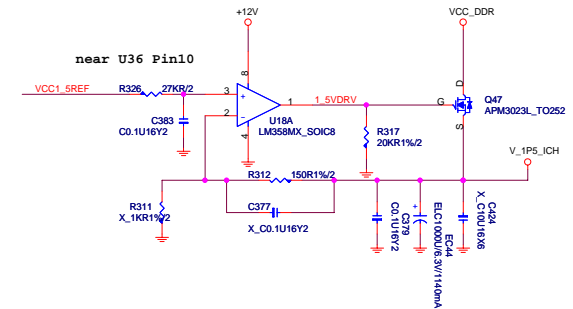
5V DIMM FOR DDR



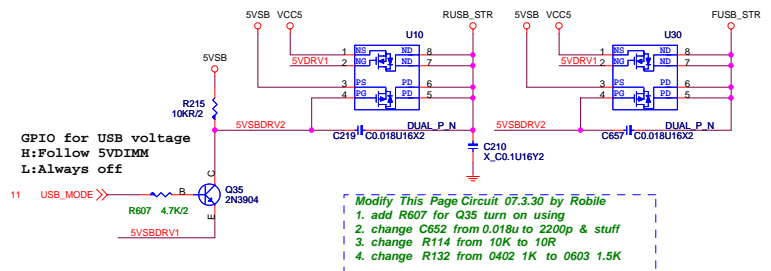
VCC1_5REF



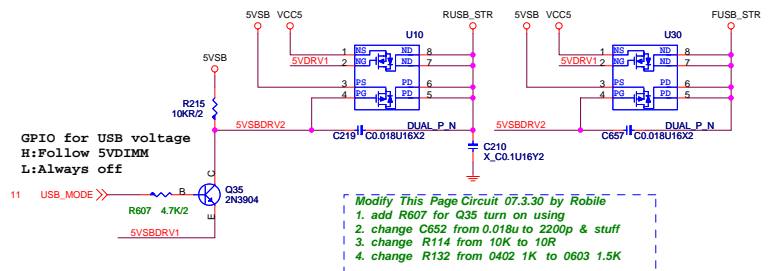
SB 1.5V 2.75A



5VSB FOR Rear USB

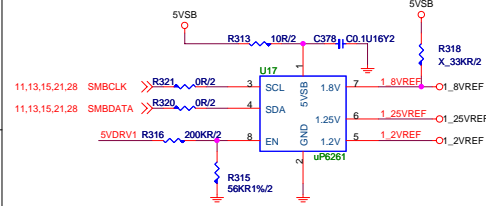


5VSB FOR Front USB

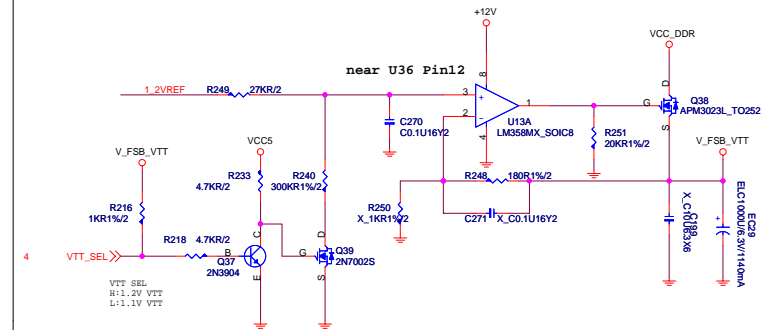


```
*Reference sinking/sourcing 100uA
*Reference ramp-up 5mS
*5VSB > 4.2V POR
*Pin8 > 1.dV Enable
*Pin8 < 0.4V Disable
```

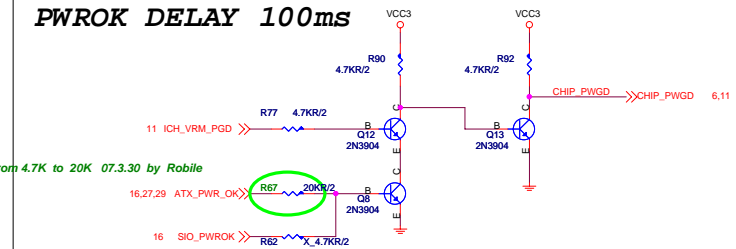
reference Voltage



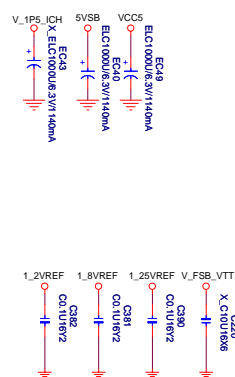
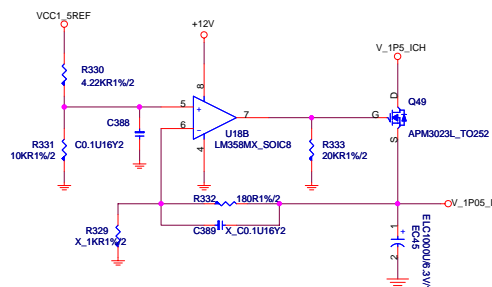
1.2V 5.8A



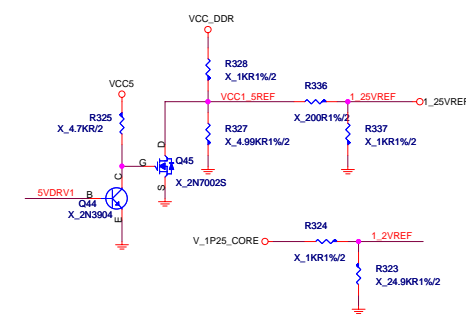
PWROK DELAY 100ms



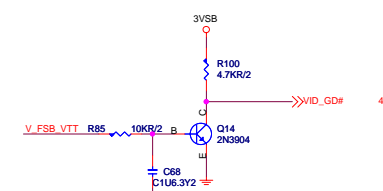
SB 1.05V 2A



```
*Reserve for remove uP6261 and uP7707
*1_8REF use uP6103's internal 0.8VREF
```



VID before PWROK >3ms

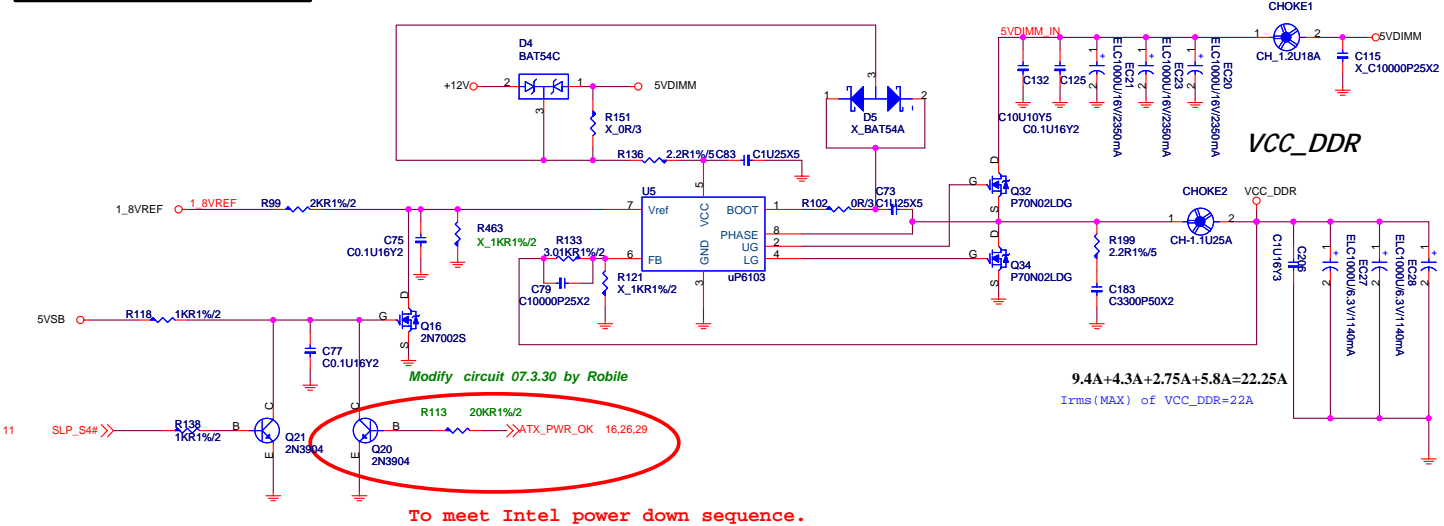


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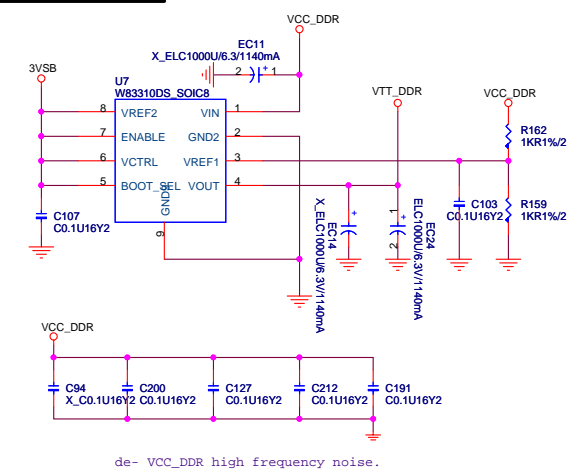
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Size Custom	Document Description ACPI controller UPI	Rev 0A
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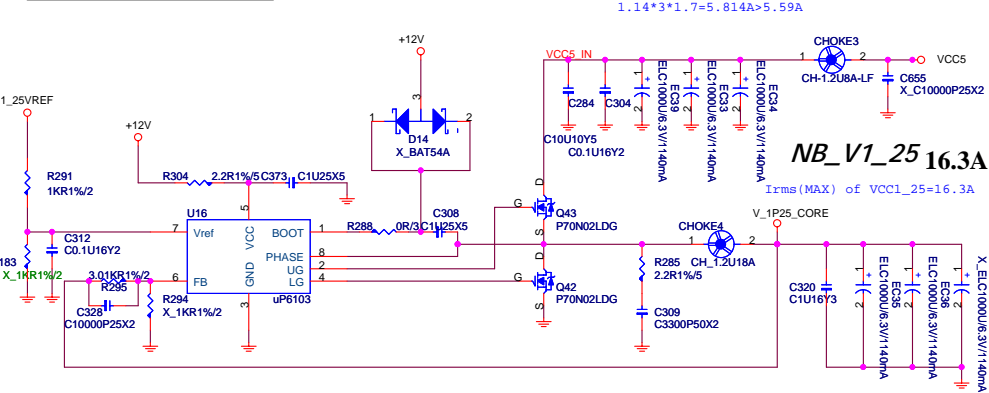
DDR II 1.8V POWER



DDR VTT Power

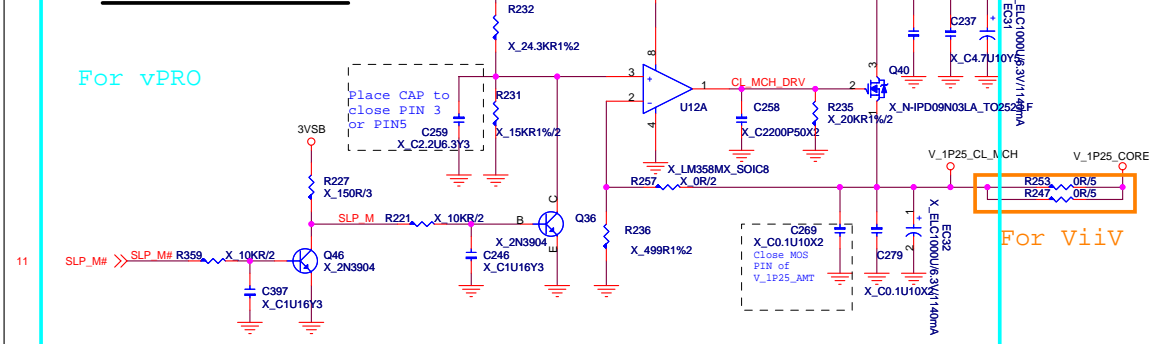


NB 1.25V POWER

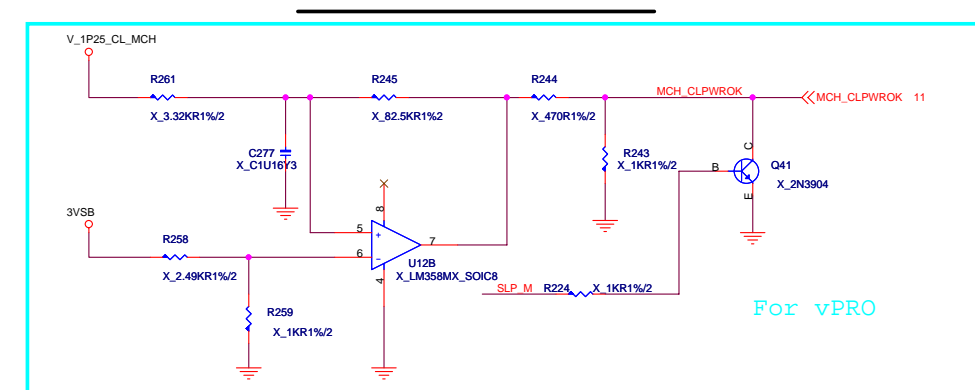


AMT POWER

V_1P25_CL_MCH (4.3A)

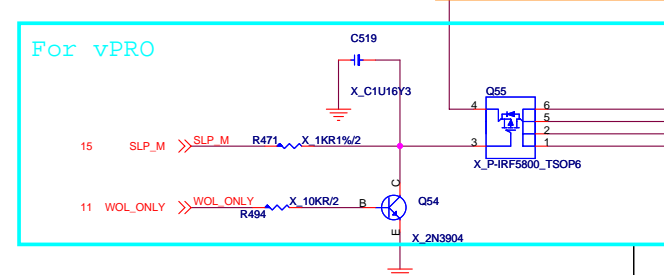


CLINK PWROK GENERATION



V_3P3_CL

(711mA)



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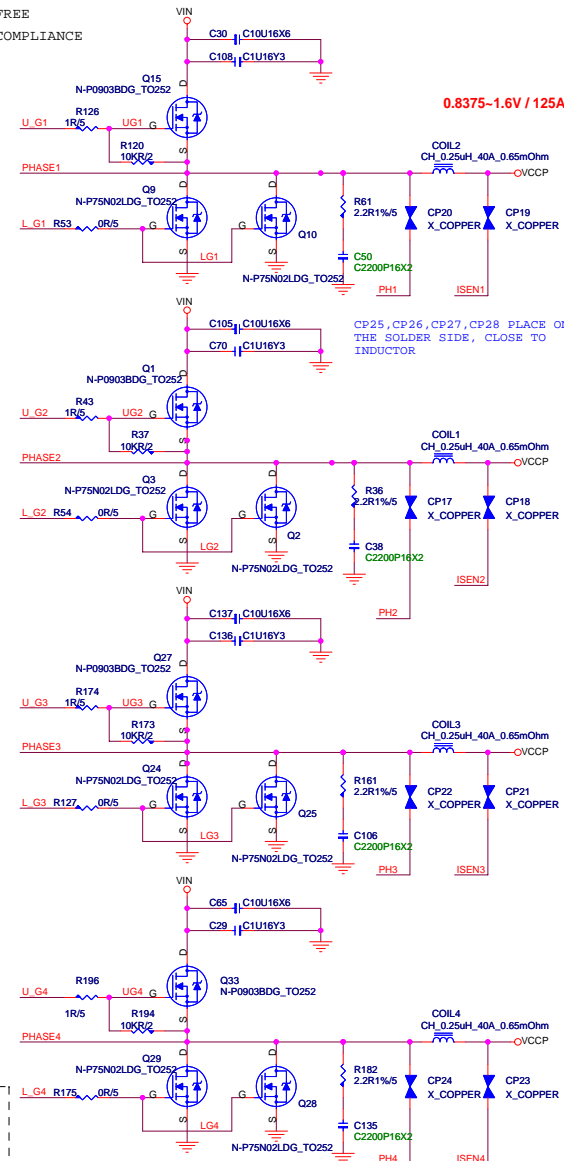
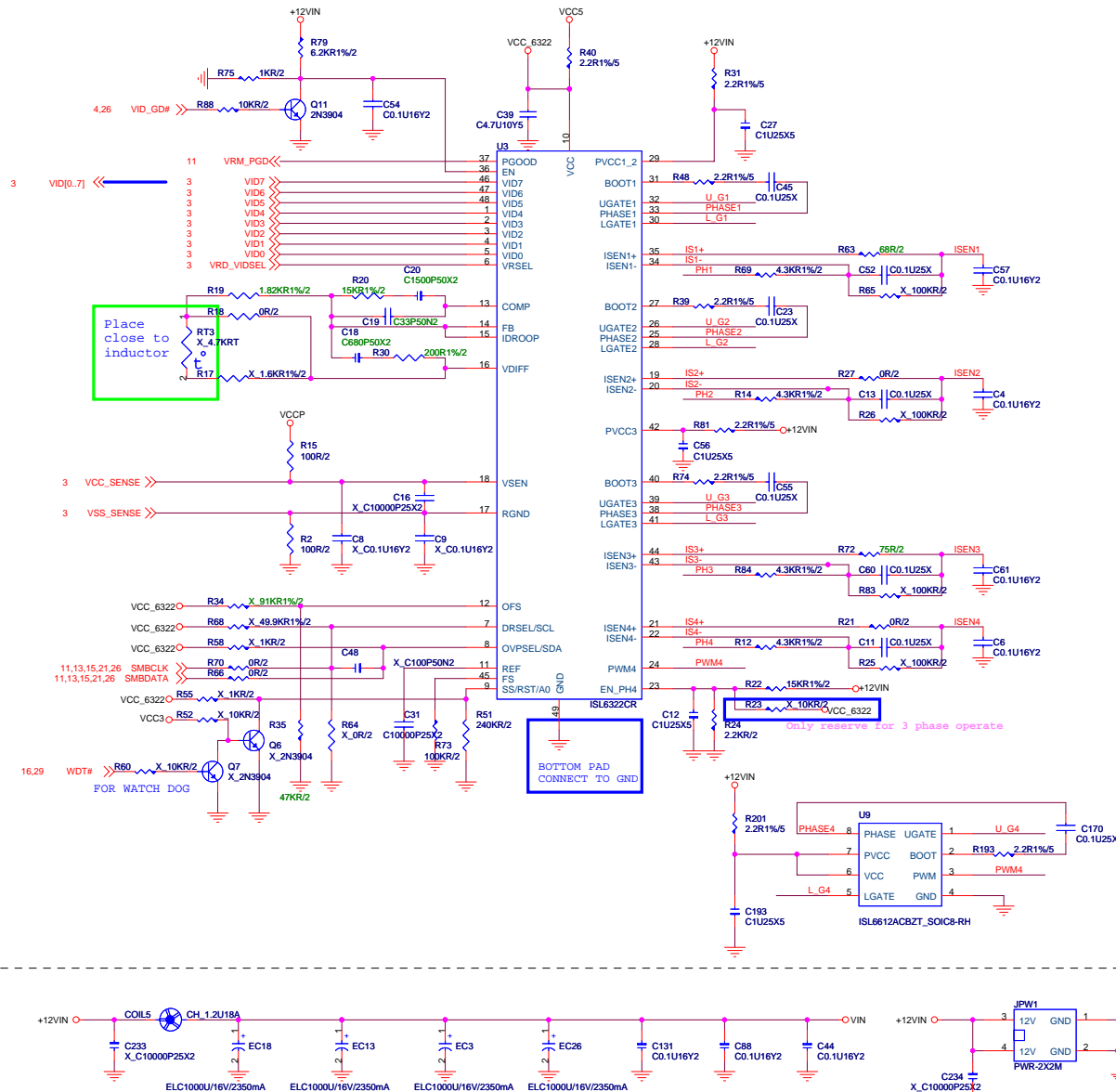
Voltage Regular Module

N-P0903BDG_TO252
P75N02LDG/TO252
C100U2SP
CD560U40S-2
1800UF/6.3V
0.25uH/40A
CH-1.1U25A-LF
CD1000U16EL20-2

mosfet/en-channel,P0903BDG,SMT/TO252,Rds(on)=9.5m (10V/25A),Vgs(on)=-1-3V,Id=50A,Ciss=1800pf,Qg=50nC,Vds=25V,Vgs= 20V,RoHS
AS06W179H-channel,P75N02LDG,SMT/TO252,Rds(on)=7m (@10V,30A),Vgs(on)=-1-3V,Id=75A,Ciss=5000pf,Qg=140nC,Vds=25V,Vgs= 20V,RoHS

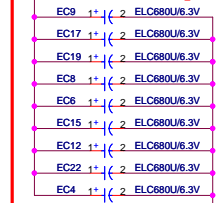
ESR compliance
ESR compliance
C30-C30L560kV47,DIP-2 8*9/3.5mm,ESR<7mohm,Ripplecur.=6100mA,Lc.=500uA,SPEC series,RoHS compliance
ESR<12m , Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs,KZJ
series
IND CHOKE,0.25uH,20%,DIP/8.5mm,40A,0.6mOhm,,PEW,FERRITE,SQUARE,RoHS COMPLIANCE
IND CHOKE,1.1uH,20%,DIP/9mm,25A,1.4mOhm,5.5T,0.9mmx3,PEW,IRON,,LEAD FREE
CAP,EL,100uF,16V,Dip-8x20/3.5mm,20%,12mOhm,2350MA,105C,3000hrs,RoHS COMPLIANCE

VIN
C30 C10U16X6



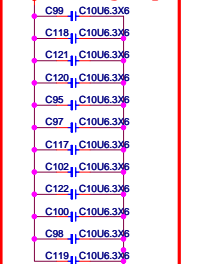
VCCP **680uF EL Capactors**

PANASONIC Cap.



MLCC Inside Socket

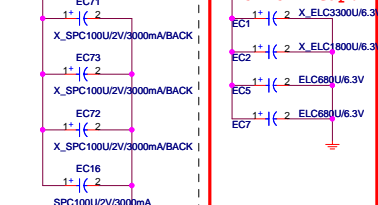
CP
b) Samsung Cap.



SP Capacitors

EL Capacitors

OSTOR Cap.

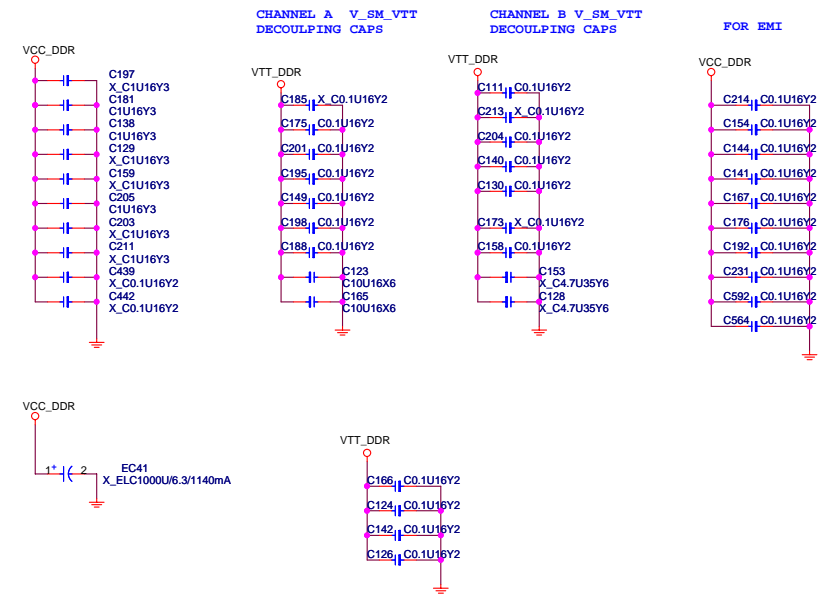
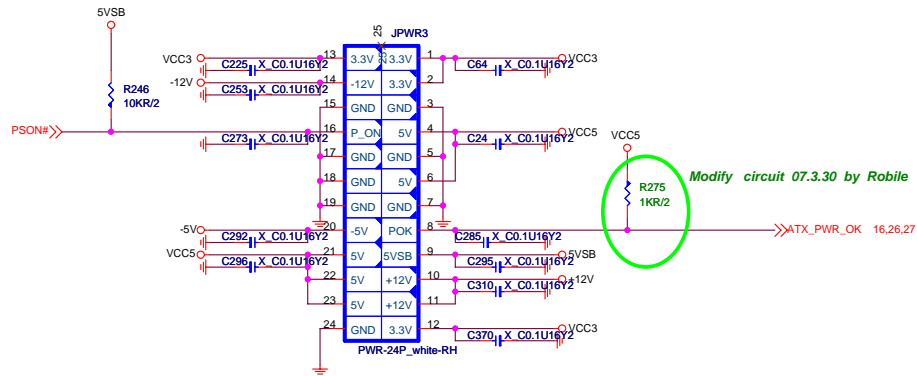


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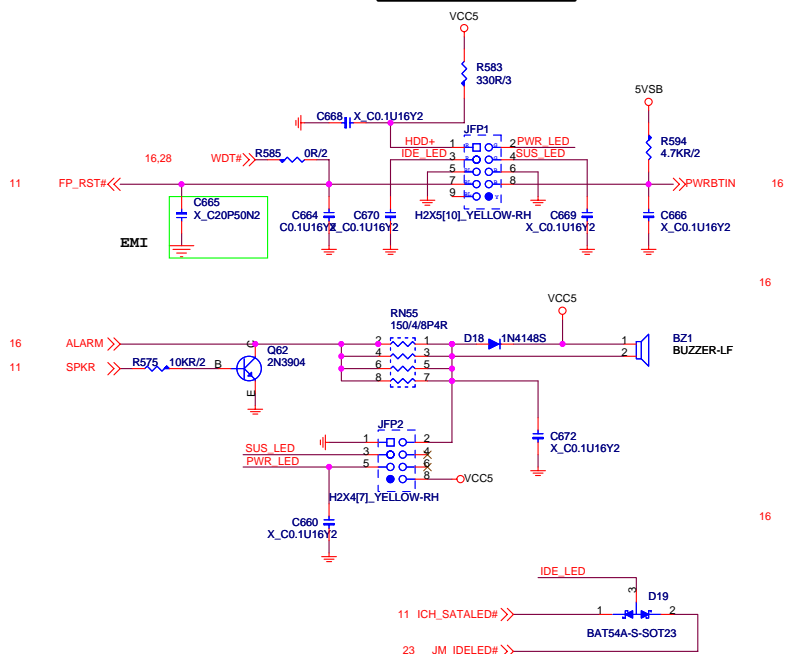
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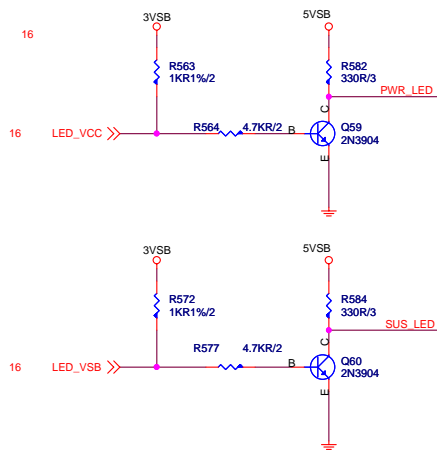
ATX POWER CONNECTOR



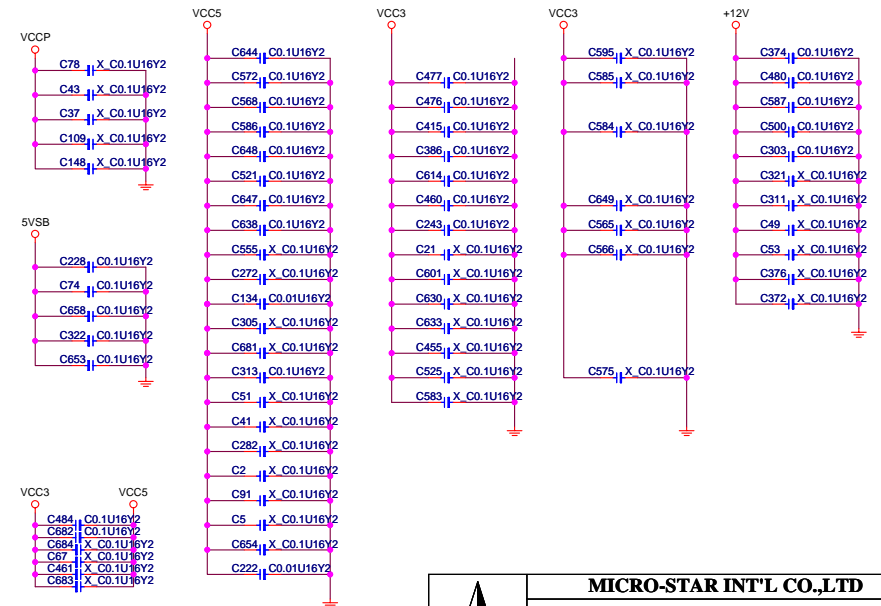
FRONT PANNEL



LED (for Fintek 71882)



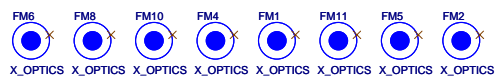
Cap. for EMI & Power



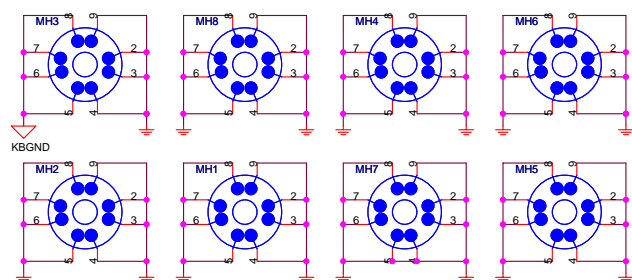
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



Simulation

